IN THE CLAIMS:

Please amend claims 2, 3, 5, and 8 and cancel claims 1, 6 and 7 as follows.

1. (Cancelled).

2. (Currently Amended) ~~The method of claim 1,~~ A method, comprising:

generating a first clock signal;

generating a plurality of clock signals, each having different phases;

generating a second clock signal based on the plurality of clock signals, the second clock signal having a different phase from the first clock signal; and

outputting the first and second clock signals,

wherein the generating a second clock uses phase interpolation.

3. (Currently Amended) ~~The method of claim 1,~~ A method, comprising:

generating a first clock signal;

generating a plurality of clock signals, each having different phases;

generating a second clock signal based on the plurality of clock signals, the second clock signal having a different phase from the first clock signal; and

outputting the first and second clock signals,

wherein the outputting outputs the first and second clock signals to a RGMII.

4. (Original) The method of claim 3, wherein the second clock signal has about a 2 ns delay with respect to the first clock signal.

5. (Currently Amended) ~~The method of claim 1~~ A method, comprising:

generating a first clock signal;

generating a plurality of clock signals, each having different phases;

generating a second clock signal based on the plurality of clock signals, the second clock signal having a different phase from the first clock signal; and

outputting the first and second clock signals,

wherein the first and second clock signals include 125 MHz clock signals.

6. (Cancelled)

7. (Cancelled)

8. (Currently Amended) A system, comprising:

means for generating a first clock signal;

means for generating a plurality of clock signals, each having different phases;

means for generating a second clock signal based on the plurality of clock signals, the second clock signal having a different phase from the first clock signal; and

means for outputting the first and second clock signals,

wherein the generating a second clock uses phase interpolation.

9. (Original) A system, comprising:

a PLL capable of generating a first clock signal;

a plurality of clock generators, communicatively coupled to the PLL, capable of generating a plurality of clock signals; and

an analog phase interpolator, communicatively coupled to the plurality of clock generators, capable of generating a second clock signal based on the plurality of clock signals, the second clock signal having a different phase from the first clock signal.

10. (Original) The system of claim 9, wherein the generating a second clock uses phase interpolation.

11. (Original) The system of claim 9, further comprising an RGMII capable of receiving the first and second clock signals.

12. (Original) The system of claim 11, wherein the second clock signal has about a 2 ns delay with respect to the first clock signal.

13. (Original) The system of claim 9, wherein the first and second clock signals include 125 MHz clock signals.

14. (Original) The system of claim 9, wherein the plurality of clock signals is based on the first clock signal.

15. (Original) The system of claim 9, wherein the plurality of signals includes eight signals.

16. (Original) A switch comprising a system according to claim 9.